RECEIVED
CENTRAL FAX CENTER
SEP 02 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	William C. Moyer *et al.*	GROUP ART UNIT:	2188
APPLN. NO.:	10/631,136	EXAMINER:	Duc T. Doan
FILED:	July 31, 2003		
TITLE:	PREFETCH CONTROL IN A DATA PROCESSING SYSTEM		

DECLARATION OF LEA HWANG LEE UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

I, Lea Hwang Lee, a resident of the city of Austin in the State of Texas, hereby state and declare as follows:

1. Currently, I am an employee of Freescale Semiconductor, Inc. in Austin, Texas.

2. I am an inventor of the invention claimed in US Patent Application 10/631,136, attorney docket number SC12888TH, along with William C. Moyer and Afzal M. Malik.

3. On April 25, 2003, a disclosure for the current Application was submitted into the Freescale Innovation Disclosure System to be scheduled for review at the first available patent committee meeting by the appropriate patent committee. A printout from this Freescale Innovation Disclosure System showing the submission date for docket number SC12888TH as April 25, 2003, is being provided as Exhibit A. A printout of the attachment PFlimit.pdf (an excerpt from the Platform Flash_BIU Block Guide V0.6 describing the

Prefetch Control and Platform Flash BIU Configuration Register) which was uploaded into the Freescale Innovation Disclosure System on April 25, 2003, is being provided as Exhibit B.

4. The disclosure for the current Application was scheduled to be presented to the Austin-Systems-Hardware Patent Committee on May 22, 2003.

5. On May 22, 2003, the disclosure for the current Application was presented to the Austin-Systems-Hardware Patent Committee, and the Austin-Systems-Hardware Patent Committee decided to pursue this disclosure as a patent.

6. On June 4, 2003, an initial meeting with patent attorney Joanna G. Chiu took place to begin preparing the current Application. A printout of the Calendar Appointment for this initial meeting is being provided as Exhibit C.

7. On July 31, 2003, the current Application was filed with the United States Patent Office.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. Executed on the date below in Austin, Texas.

Respectfully submitted,

8/25/05

Date

Lea Hwang Lee

Applicant

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	William C. Moyer *et al.*	GROUP ART UNIT:	2188
APPLN. NO.:	10/631,136	EXAMINER:	Doc T. Doan
FILED:	July 31, 2003		
TITLE:	PREFETCH CONTROL IN A DATA PROCESSING SYSTEM		

DECLARATION OF AFZAL M. MALIK UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

I, Afzal M. Malik, a resident of the city of Austin in the State of Texas, hereby state and declare as follows:

1. At the time of filing the current Application, I was an employee of Motorola, Inc.'s Semiconductor Products Sector in Austin, Texas, which later became Freescale Semiconductor, Inc.

2. I am an inventor of the invention claimed in US Patent Application 10/631,136, attorney docket number SC12888TH, along with William C. Moyer and Lea Hwang Lee.

3. On April 25, 2003, a disclosure for the current Application was submitted into the Freescale Innovation Disclosure System to be scheduled for review at the first available patent committee meeting by the appropriate patent committee. A printout from this Freescale Innovation Disclosure System showing the submission date for docket number SC12888TH as April 25, 2003, is being provided as Exhibit A. A printout of the attachment PFlimit.pdf (an excerpt from the Platform Flash_BIU Block Guide V0.6 describing the

Prefetch Control and Platform Flash BIU Configuration Register) which was uploaded into the Freescale Innovation Disclosure System on April 25, 2003, is being provided as Exhibit B.

4. The disclosure for the current Application was scheduled to be presented to the Austin-Systems-Hardware Patent Committee on May 22, 2003.

5. On May 22, 2003, the disclosure for the current Application was presented to the Austin-Systems-Hardware Patent Committee, and the Austin-Systems-Hardware Patent Committee decided to pursue this disclosure as a patent.

6. On June 4, 2003, an initial meeting with patent attorney Joanna G. Chiu took place to begin preparing the current Application. A printout of the Calendar Appointment for this initial meeting is being provided as Exhibit C.

7. On July 31, 2003, the current Application was filed with the United States Patent Office.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. Executed on the date below in Austin, Texas.

Respectfully submitted,

Aug 25, 2005
Date

Afzal Malik
Afzal M. Malik
Applicant

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	William C. Moyer *et al.*	GROUP ART UNIT:	2188
APPLN. NO.:	10/631,136	EXAMINER:	Duc T. Doan
FILED:	July 31, 2003		
TITLE:	PREFETCH CONTROL IN A DATA PROCESSING SYSTEM		

DECLARATION OF WILLIAM C. MOYER UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

I, William C. Moyer, a resident of the city of Dripping Springs in the State of Texas, hereby state and declare as follows:

1. Currently, I am an employee of Freescale Semiconductor, Inc. in Austin, Texas.

2. I am an inventor of the invention claimed in US Patent Application 10/631,136, attorney docket number SC12888TH, along with Lea Hwang Lee and Afzal M. Malik.

3. On April 25, 2003, I submitted a disclosure for the current Application into the Freescale Innovation Disclosure System to be scheduled for review at the first available patent committee meeting by the appropriate patent committee. A printout from this Freescale Innovation Disclosure System showing the submission date for docket number SC12888TH as April 25, 2003, is being provided as Exhibit A. A printout of the attachment PFlimit.pdf (an excerpt from the Platform Flash_BIU Block Guide V0.6 describing the

Prefetch Control and Platform Flash BIU Configuration Register) which was uploaded into the Freescale Innovation Disclosure System on April 25, 2003, is being provided as Exhibit B.

4. The disclosure for the current Application was scheduled to be presented to the Austin-Systems-Hardware Patent Committee on May 22, 2003.

5. On May 22, 2003, I presented the disclosure for the current Application to the Austin-Systems-Hardware Patent Committee, and the Austin-Systems-Hardware Patent Committee decided to pursue this disclosure as a patent.

6. On June 4, 2003, an initial meeting with patent attorney Joanna G. Chiu took place to begin preparing the current Application. A printout of the Calendar Appointment for this initial meeting is being provided as Exhibit C.

7. On July 31, 2003, the current Application was filed with the United States Patent Office.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. Executed on the date below in Austin, Texas.

Respectfully submitted,

Aug. 25, 2005
Date

William C. Moyer
Applicant

freescale semiconductor

eIntelligence - Inn

Disclosure SC12888TH (19435)

ID: SC12888TH (19435)
Title: Fine-grained Prefetch Limit Control for a Memory System Controller

Innovators: Bill Moyer, Lea Hwang Lee, Afzal M. Malik
Status: Filed
Status Date: 22 May 2003 10:30 AM
Disposition: Pursue
Submitted Date: 25 Apr 2003
Review Date: 22 May 2003 10:30 AM
Sector: SPS
Patent Committee: Austin - Systems - Hardware
Business Unit: Networking and Computing Systems Group
Organization: SPS, NCSG, NCSG TSS, PERF SOC
Department: RU433
Location: TX32
Submit Country: USA

Workflow

Role	Name	Action
First Innovator	Bill Moyer	Verification Complete 4/25/2003
Co-Innovator	Lea Hwang Lee	Verification Complete 6/10/2003
Co-Innovator	Afzal M. Malik	Verification Complete 6/3/2003
Witness	John Arends	Acknowledgement Complete 4/25/2003, Noteb
Witness	Jeff Scott	Acknowledgement Complete 4/25/2003, Noteb
Manager	Dan Cronin	Acknowledgement Complete 4/28/2003

Reviewer Information

Role	Name	Action
Grading Results		

Documents

	Document Name	Description	Document Type	Uploaded By	Uploaded
	PFlimit.pdf		Unspecified		25 Apr 2(
	SC12888TH.1.pdf	Disclosure presentation	Unspecified		22 May 2

Exhibit B

Section 3 PFBIU Registers

RELEVANT CONTROL FOR THE INNOVATION IS HIGHLIGHTED IN RED..

3.1 Overview

There are two registers that control operation of the PFBIU. These registers should only be read from or written to with a 32-bit access.

3.2 Prefetch Control

Several algorithms are available for prefetch control which trade off performance for power. They are described in **3.2 Platform Flash BIU Configuration Register - (PFBCR)**. More aggressive prefetching increases power due to the number of wasted (discarded) prefetches, but may increase performance by lowering average read latency.

3.3 Platform Flash BIU Configuration Register - (PFBCR)

The PFBIU Configuration register (PFBCR) is used to configure operation of the PFBIU. The register is described below.

Table 3-1 PFBIU Configuration Register (PFBCR) Summary

PFBCR													FlashRegs_Base + 0x0??				
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NAME	M15 PFE	M14 PFE	M13 PFE	M12 PFE	M11 PFE	M10 PFE	M9 PFE	M8 PFE	M7 PFE	M6 PFE	M5 PFE	M4 PFE	M3 PFE	M2 PFE	M1 PFE	M0 PFE
TYPE	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	APC			WWSC		RWSC			DPFEN		IPFEN	PFLIM				BFEN
TYPE	rw			rw		rw			rw		rw	rw				rw
RESET	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Table 3-2 PFBIU Configuration Register Field Descriptions

Name	Description	Settings
M15PFE **M14PFE** **M13PFE** .. **M0PFE** **Bits 31:16**	**Master X Prefetch enable** - These bits are used to control whether prefetching may be triggered based on the master ID of a requesting master. These bits are cleared by hardware reset.	0 - No prefetching may be triggered by this master 1 - Prefetching may be triggered by this master
APC **Bits 15:13**	**Address Pipelining Control** - This field is used to control the number of cycles between pipelined access requests. This field must be set to a value corresponding to the operating frequency of the PFBIU. The required settings are documented in the SoC specification. Higher operating frequencies require non-zero settings for this field for proper Flash operation. This field is set to 3'b111 by hardware reset.	000 - Accesses may be pipelined back-to-back 001 - Access requests require one additional hold cycle 010 - Access requests require two additional hold cycles ... 110 - Access requests require six additional hold cycles 111 - No address pipelining
WWSC **Bits 12:11**	**Write Wait State Control** - This field is used to control the number of wait-states to be added to the best-case Flash array access time for Flash array writes. This field must be set to a value corresponding to the operating frequency of the PFBIU. The required settings are documented in the SoC specification. Higher operating frequencies require non-zero settings for this field for proper Flash operation. This field is set to 2'b11 by hardware reset.	00 - No additional wait-states are added 01 - One additional wait-state is added 10 - Two additional wait-states are added 11 - Three additional wait-states are added
RWSC **Bits 10:8**	**Read Wait State Control** - This field is used to control the number of wait-states to be added to the best-case Flash array access time for Flash array reads. This field must be set to a value corresponding to the operating frequency of the PFBIU. The required settings are documented in the SoC specification. Higher operating frequencies require non-zero settings for this field for proper Flash operation. This field is set to 3'b111 by hardware reset.	000 - No additional wait-states are added 001 - One additional wait-state is added ... 111 - Seven additional wait-states are added
DPFEN **Bit 7:6**	**Data Prefetch Enable** - This field enables or disables prefetching initiated by a data read access. This field is cleared by hardware reset.	00 - No prefetching is triggered by a data read access 01 - Prefetching may be triggered only by a data burst read access 10 - Reserved 11 - Prefetching may be triggered by any data read access

Table 3-2 PFBIU Configuration Register Field Descriptions

Name	Description	Settings
IPFEN **Bit 5:4**	**Instruction Prefetch Enable** - This bit enables or disables prefetching initiated by an instruction read access. This field is cleared by hardware reset.	00 - No prefetching is triggered by an instruction read access 01 - Prefetching may be triggered only by an instruction burst read access 10 - Reserved 11 - Prefetching may be triggered by any instruction read access
PFLIM **Bits 3:1**	**PFBIU Prefetch Limit** - This field controls the prefetch algorithm used by the PFBIU prefetch controller. This field defines a limit on the maximum number of sequential prefetches which will be attempted between buffer misses. This field is cleared by hardware reset.	000 - No prefetching is performed 001 - A single additional line (next sequential) is prefetched on a Buffer Miss 010 - Up to two additional lines may be prefetched following each Buffer Miss before prefetching is halted. A single additional line (next sequential) is prefetched on a Buffer Miss, and the next sequential line is prefetched on a Buffer Hit (if not already present). 011 - Up to three additional lines may be prefetched following each Buffer Miss before prefetching is halted. Only a single additional prefetch is initiated after each Buffer hit or miss. 100 - Up to four additional lines may be prefetched following each Buffer Miss before prefetching is halted. Only a single additional prefetch is initiated after each Buffer hit or miss. 101 - Up to five additional lines may be prefetched following each Buffer Miss before prefetching is halted. Only a single additional prefetch is initiated after each Buffer hit or miss. 110 - An unlimited number of additional lines may be prefetched following each Buffer Miss. Only a single additional prefetch is initiated on each Buffer hit or miss. 111 - Reserved

Table 3-2 PFBIU Configuration Register Field Descriptions

Name	Description	Settings
BFEN **Bit 0**	**PFBIU Line Read Buffers Enable** - This bit enables or disables line read buffer hits. It is also used to invalidate the buffers. This bits is cleared by hardware reset.	0 - The line read buffers are disabled from satisfying read requests, and all buffer valid bits are cleared. 1 - The line read buffers are enabled to satisfy read requests on hits. Buffer valid bits may be set when the buffers are successfully filled.

Exhibit C

Cox Elaine-ra5685

Subject:	SC12888TH DAC MOYER/JGC/TB
Location:	SWEETWATER CONFERENCE ROOM
Start:	Wed 6/4/2003 8:30 AM
End:	Wed 6/4/2003 5:00 PM
Recurrence:	(none)